UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,244	03/11/2004	Guido Gabriele Albasini	851863.412	3549

38106 7590 05/16/2005

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVENUE, SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/798,244	ALBASINI ET AL.
	Examiner	Art Unit
	Linh M. Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 9-12* is/are rejected.

7)☒ Claim(s) *3-8, 13-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-19 are presented in the instant application according to the Applicants' filing on 03/11/2004.

Remarks

Note that claims 1-13 and 15-20 have been renumbered as 1-19 since claim 14 was missing.

Inventorship

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim Objections/Minor Informalities

2. Claim 11 is objected to because of the following informalities:

Claim 11, line 11, it is suggested to change "if" to --when-- to reflect positive limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1, 2 and 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Magazz' et al. (U.S. Patent No. 6,593,817, of record).

With respect to claim 1, Magazz' et al. discloses, in Fig. 11, a phase-locked loop circuit for providing an output signal [from VCO] having a frequency depending on the frequency of a reference signal [Sref], the circuit comprising a) mean for deriving [12] a feedback signal from the output signal, b) means for providing [8] a control signal indicative of a phase difference between the reference signal [Sref] and the feedback signal [Sdiv], c) means for controlling [VCO] the frequency of the output signal according to the control signal and d) means for conditioning [14, 16, 17] the control signal through a conditioning signal [output from 9], wherein the means for conditioning includes means for accumulating energy [14] provided by the control signal and the conditioning signal during a first phase and for transferring [SW2] the accumulated energy to the means for controlling the frequency of the output signal during a second phase.

With respect to claim 2, Magazz' et al. discloses, in Fig. 11, that the means for conditioning includes capacitive means [14], first switching means [SW1] responsive to a first enabling signal for coupling the capacitive means with the mean for providing the control signal

during the first phase, and second switching means [SW2] responsive to a second enabling signal for coupling the capacitive means with the means for controlling the frequency of the output signal during the second phase.

With respect to claim 9, Magazz' et al. discloses, in Fig. 11, that the means for conditioning includes means for providing a second conditioning signal [lock] for causing the circuit to enter a lock condition when the reference signal and the feedback signal have the same frequency and a pre-defined phase difference, the control signal consisting of a series of pulses and the second conditioning signal having constant amplitude corresponding to the pre-defined phase difference.

With respect to claim 10, Magazz' et al. discloses, in Fig. 11, a circuit and its corresponding method of providing an output signal having a frequency depending on the frequency of a reference signal [Sref], the method comprising the steps of a) deriving a feedback signal from the output signal [from VCO], b) providing [8] a control signal indicative of a phase difference between the reference signal [Sref] and the feedback signal [Sdiv], c) controlling [VCO] the frequency of the output signal according to the control signal, and d) conditioning [14, 16, 17] the control signal through a conditioning signal [output from 9], wherein accumulating [14] energy provided by the control signal and the conditioning signal during the first phase, and transferring [SW2] the accumulated energy for controlling the frequency of the output signal during a second phase.

With respect to claim 11, Magazz' et al. discloses, in Fig. 11, a phase-locked loop circuit for providing an output signal having a frequency depending on the frequency of a reference signal, the circuit comprising a) a charge pump generator [9] including an output terminal, b) a

signal filter [10]; and c) a first compensation circuit [14, 16, 17] connected to an intermediate node between the output terminal of the charge pump generator and the signal filter, the first compensation circuit including a plurality of energy storage legs connected to the intermediate node and controlled by respective bits of a digital compensation signal, each energy storage leg being structured to store charge during a first phase when the bit controlling the energy storage leg is active and output the stored charge during a second phase.

With respect to claim 12, Magazz' et al. discloses, in Fig. 11, that the first compensation circuit further includes a first capacitor [14] connected between the energy storage legs and the intermediate node.

Allowable Subject Matter

5. Claims 3-8, 13 and 14-19 (renumbered 15-20) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest:

a) A phase-locked loop circuit, which is of the fractional type for synthesizing the output signal multiplying the frequency by the reference signal by a fractional conversion factor, the means for deriving the feedback signal including means for dividing the frequency of the output signal a dividing ratio being modulated to provide the conversion factor on the average, and the means for conditioning includes means for providing a first conditioning signal for compensating a phase error caused by the modulation of the dividing ratio, the control signal consisting of a series of pulses modulated according to a first technique and the first conditioning signal

consisting of a series of pulses modulated according to a second technique, as called for in claim 3;

b) A phase-locked loop circuit, in which the first compensation circuit further includes an amplifier connected between the energy storage legs and the intermediate node, the first capacitor being connected between an input and an output of the amplifier, as called for in claim 13;

c) A phase-locked loop circuit, in which the first compensation circuit further includes a first switch connected between the output of the charge pump and a first plate of the first capacitor, as called for in claim 14 (renumbered 15);

d) A phase-locked loop circuit, in which each energy storage leg includes an AND gate having a first input receiving the respective bit of the digital compensation signal, a second input receiving a phase control signal, and an output connected to a control terminal of a switch, as called for in claim 16 (renumbered 17); and

e) A phase-locked loop circuit further includes a second compensation circuit being connected between the output of the charge pump and the signal filter, the second compensation circuit including a first energy storage element, as called for in claim 17 (renumbered 18).

Citation of Relevant Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Kasahara et al. (U.S. Patent No. 6,714,772) discloses a phase locked loop circuit capable of processing two or more transmit and receive signal different in frequency band.

Prior art Segawa et al. (U.S. Patent No. 6,342,818) discloses a phase locked loop having switching circuit for maintaining lock during loss of input signal.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER